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Efficient associative computation with memristive synapses

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Neural associative networks are a promising computational paradigm, both for modeling neural circuits of the brain and implementing large scale cognitive systems based on associative computation and Hebbian cell assemblies [1]. Previous works have extensively investigated optimal synaptic learning in associative networks assuming linear models of the Hopfield-type [2] or simple non-linear models of the Steinbuch/Willshaw-type [3]. We have recently developed a unifying framework of Bayesian associative learning [4] and developed efficient discretizations thereof [5]. One surprising result of these studies is that, if employing an appropriate synaptic learning rule, low precision or even binary synapses have almost the same computational capacities as real-valued synapses employing Bayesian learning.

On the other hand, there are recent developments of imprecise analog electric storage elements that allow activity depend modification of resistance in a similar way as synapses modify synaptic strength [6]. These so-called memristors allow nanoscale integration and promise to make neuromorphic hardware much more efficient in terms of space and energy compared to digital VLSI. For example, it may become possible to implement individual synapses with single memristors each embodying analog synaptic computation and learning. By contrast, current digital neuromorphic hardware suffers from a "synaptic bottleneck" because each synapse requires many circuit elements to realize local learning and memory [7].

This simulation study investigates neural associative networks with different memristor-based synapses using the model of Strukov and colleagues [6]. Specifically, we simulated different types of completely connected feed-forward networks of two neuron populations u and v (sizes m=1000, n=300). The task was to learn a set of M memory associations between address patterns u^μ and content patterns v^μ, where memory patterns correspond to binary activity vectors (10% active units). After learning, we tested retrieval by activating noisy address patterns (50% noise) and comparing the resulting output with the original content patterns. Pattern capacity M_ε was estimated from the maximal M that keeps output noise level below ε=10% (where the Baysian capacity bound is at $M_{0.1}\approx 320$ for the described parameters [4]).

In a first approach we modeled Steinbuch-type networks of binary synapses where coincident presynaptic and postsynaptic activity drives memristors into saturation. Such implementations are straight-forward, but result in a relatively low storage capacity ($M_{0.1}\approx 70$) as expected from theory [3].

Second, we tried to implement optimal linear learning by driving memristors at a linear working point where each pre-/postsynaptic pairing increases conductance by a fixed amount. However, as confirmed by a theoretical analysis, such networks can implement only trivial linear learning rules and achieve only very low capacity ($M_{0.1}\approx 15$).

In the final approach, we modeled each synapse by a memristor and an additional Zener diode-type element to prevent leakage currents. With this and a dedicated pre-/postsynaptic signaling it becomes possible to approximate optimal linear covariance learning and to reach a much higher storage capacity ($M_{0.1}\approx 150$). Surprisingly, capacity can be significantly increased if, in a subsequent learning stage, the strongest and weakest synapses are driven to maximal and minimal conductances, respectively ($M_{0.1}\approx 200$).

Such thresholding of conductances leaves the memristors much more robust against noise during retrieval operation and the resulting capacity is virtually equivalent to the capacity for optimal binarization of synaptic strengths obtained from Bayesian learning ($M_{0.1}\approx 205$) [4].

Thus, our results show that memristor-based networks can, in principle, implement efficient associative computation. This encourages further investigation of memristor-based hardware realizations of neural networks and the design of corresponding general purpose large-scale architectures for associative computation.

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